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**1 A 10-b 75-MSPS subranging A/D converter with integrated sample hold**

*Petschacher, R.; Zojer, B.; Astegher, B.; Jessner, H.; Lechner, A.;*  
 Solid-State Circuits, IEEE Journal of , Volume: 25 , Issue: 6 , Dec. 1990  
 Pages:1339 - 1346

[\[Abstract\]](#)    [\[PDF Full-Text \(676 KB\)\]](#)    **IEEE JNL**
**2 A 75 mW 10 b 20 MSample/s CMOS subranging ADC with 59 dB SNR**

*Brandt, B.; Lutsky, J.;*  
 Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999  
 IEEE International , 15-17 Feb. 1999  
 Pages:322 - 323

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